## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-18. (Canceled)

19. (Currently Amended) A method performed in response to execution of a first instruction, comprising:

storing only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage ~~locations in response to execution of a~~ locations in response to the execution of the first instruction, in which the first instruction ~~that does not specify an has an order in which~~ implicitly indicates that the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations; and

duplicating bits from the plurality of non-contiguous groups of source bits ~~destination storage locations~~ into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations in response to the execution of the first instruction which implicitly indicates that the plurality of non-contiguous groups of source bits are to be duplicated.

20. (Previously Presented) The method of claim 19 in which the source bits are stored in a first register.

21. (Cancelled)

22. (Previously Presented) The method of claim 19 in which the source bits are stored in a first memory location.

23. (Currently Amended) The method of claim 19 in which the source bits represent ~~represent a~~ single-precision floating point values ~~value~~.

24-92. (Canceled)

93. (Currently Amended) An apparatus comprising:

a first storage area to store a plurality of non-contiguous groups of source bits ~~in response to execution of a first instruction~~; and

a core coupled with the first storage area, the core in response to execution of a first instruction ~~a second storage area~~ to store only the plurality of non-contiguous groups of source bits which are implicitly indicated by the instruction into a plurality of non-contiguous groups of destination storage locations and to store ~~contiguous~~ duplicates of the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations.

94. (Currently Amended) The apparatus of claim 93, wherein the plurality of non-contiguous groups of source bits are to represent a plurality of 32-bit single-precision ~~double-precision~~ floating point values ~~value~~.

95. (Previously Presented) The apparatus of claim 94, wherein the first storage area comprises a 128-bit memory location.

96. (Currently Amended) The apparatus of claim 94, wherein the first storage area comprises ~~and second storage areas each comprise~~ a 128-bit register.

97. (Currently Amended) The apparatus of claim 93, wherein the plurality of non-contiguous groups of source bits comprises ~~comprise~~ four single-precision floating point values.

98. (Currently Amended) The apparatus of claim 93, wherein the second storage area is to store only two ~~of the plurality of~~ non-contiguous groups of source bits and their duplicates.

99-100. (Cancelled)

101. (Currently Amended) A system comprising:

a memory to store a plurality of instructions;

a processor to fetch a first instruction from the memory, wherein the first instruction, if executed by the processor, is to cause the processor to store only a plurality of non-contiguous groups of source bits which are not explicitly specified through the first instruction into a plurality of non-contiguous groups of destination storage locations and to store ~~contiguous~~ duplicates of the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations.

102. (Currently Amended) The system of claim 101, wherein the plurality of non-contiguous groups of source bits include a least significant group of 32 source bits.

103. (Currently Amended) The system of claim 101, wherein the plurality of non-contiguous groups of source bits include a most significant group of 32 source bits.

104. (Previously Presented) The system of claim 102, wherein the plurality of non-contiguous groups of source bits include a second most significant group of 32 source bits.

105. (Previously Presented) The system of claim 103, wherein the plurality of non-contiguous groups of source bits include a second least-significant group of 32 source bits.

106. (Canceled)

107. (Previously Presented) The system of claim 105, wherein the first instruction is a MOVSHDUP instruction.

108. (Previously Presented) The system of claim 104, wherein the first instruction is a MOVSLDUP instruction.

109. (Currently Amended) The system of claim 101, wherein the processor is to fetch a second instruction from the memory, the second instruction to cause the processor to store a first number of non-contiguous duplicates of a second number of contiguous groups of source bits into a destination storage location, the first number being larger than the second number.

110. (Currently Amended) A ~~machine-readable~~ medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction ~~an instruction~~, which if executed by ~~a machine~~ the processor, causes the processor ~~machine~~ to perform a method comprising:

storing bits [31-0] of a source value into bit storage locations [63-32] and [31-0] of a destination register;

storing bits [95-64] of the source value into bit storage locations [127-96] and [95-64] of the destination register, wherein the instruction implicitly indicates the bits of the source value which ~~does not include a code to designate the order in which the source bits~~ are to be stored in the destination register.

111. (Currently Amended) The ~~machine-readable~~ medium of claim 110 wherein the source value is stored in a memory location.

112. (Currently Amended) The ~~machine-readable~~ medium of claim 110, wherein the source value is stored in a register.

113. (Currently Amended) A ~~machine-readable~~ medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction ~~an instruction~~, which if executed by ~~a machine~~ the processor causes the processor ~~machine~~ to perform a method comprising:

storing bits [63-32] of a source value into bit storage locations [31-0] and [63-32] of a destination register;

storing bits [127-96] of the source value into bit storage locations [127-96] and [95-64] of the destination register, wherein the instruction implicitly indicates the bits of the source value which ~~does not include a code to designate the order in which the source bits~~ are to be stored in the destination register.

114. (Currently Amended) The ~~machine-readable~~ medium of claim 113 wherein the source value is stored in a memory location.

115. (Currently Amended) The ~~machine-readable~~ medium of claim 113, wherein the source value is stored in a register.

116. (Currently Amended) A ~~machine-readable~~ medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction ~~an instruction~~, which if executed by ~~a machine~~ the processor causes the processor ~~machine~~ to perform a method comprising:

storing only bits [63-32] of a source value into bit storage locations [127-96] and [63-32] of a destination register;

storing only bits [31-0] of the source value into bit storage locations [31-0] and [95-64] of the destination register, wherein the instruction implicitly indicates the bits of the source value which ~~does not include a code to designate the order in which the source bits~~ are to be stored in the destination register.

117. (Currently Amended) The ~~machine-readable~~ medium of claim 116 wherein the source value is stored in a memory location.

118. (Currently Amended) The ~~machine-readable~~ medium of claim 116, wherein the source value is stored in a register.

119. (Currently Amended) A ~~machine-readable~~ medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction ~~an instruction~~, which if executed by ~~a machine~~ the processor, causes the processor ~~machine~~ to perform a method comprising:

storing bits [31-0] of a source value into bit storage locations [31-0] of a destination register;

duplicating bits from the bit storage locations [31-0] to bit storage locations [63-32] of the destination register;

storing bits [95-64] of the source value into bit storage locations [95-64] of the destination register; and

duplicating bits from the bit storage locations [95-64] to bit storage locations [127-96] of the destination register, wherein the instruction implicitly indicates the bits of the source value which ~~does not include a code to designate the order in which the source bits~~ are to be stored in the destination register.

120. (Currently Amended) A ~~machine-readable~~ medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction ~~an instruction~~, which if executed by ~~a machine~~ the processor causes the processor ~~machine~~ to perform a method comprising:

storing bits [63-32] of a source value into bit storage locations [63-32] of a destination register;

duplicating bits from the bit storage locations [63-32] to bit storage locations [31-0] of the destination register;

storing bits [127-96] of the source value into bit storage locations [127-96] of the destination register; and

duplicating bits from the bit storage locations [127-96] to bit storage locations [95-64] of the destination register, wherein the instruction implicitly indicates the bits of the source value which ~~does not include a code to designate the order in which the source bits~~ are to be stored in the destination register.

121. (Previously Presented) The method of claim 19, wherein the order in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations is fixed.

122. (Previously Presented) The method of claim 19, wherein the order in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations is specific in accordance with the first instruction.

123. (Currently Amended) The method of claim 19, wherein the first instruction is associated with one single unique order ~~order of~~ in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations.

124. (New) The apparatus of claim 93, in which the first instruction indicates operands consisting of a single source operand corresponding to the source bits and a single destination operand corresponding to the destination storage locations.

125. (New) The medium of claim 110, in which the first instruction indicates operands consisting of a single source operand corresponding to the source value and a single destination operand corresponding to the destination register.

126. (New) The medium of claim 113, in which the first instruction indicates operands consisting of a single source operand corresponding to the source value and a single destination operand corresponding to the destination register.

127. (New) The medium of claim 116, in which the first instruction indicates operands consisting of a single source operand corresponding to the source value and a single destination operand corresponding to the destination register.

128. (New) The apparatus of claim 93, in which the plurality of non-contiguous groups of source bits are fixed by the first instruction.

129. (New) The medium of claim 110, in which the bits of the source value to be stored in the destination register are fixed for the instruction.

130. (New) The medium of claim 113, in which the bits of the source value to be stored in the destination register are fixed for the instruction.

131. (New) The medium of claim 116, in which the bits of the source value to be stored in the destination register are fixed for the instruction.

132. (New) The medium of claim 110, wherein the medium comprises a memory.

133. (New) The medium of claim 113, wherein the medium comprises a memory.

134. (New) The medium of claim 116, wherein the medium comprises a memory.

135. (New) An apparatus comprising:

a register to store source bits;

a core coupled with the register, the core in response to execution of a first instruction to store a plurality of non-contiguous groups of the source bits, which are not explicitly specified through the

first instruction, into a plurality of non-contiguous groups of destination storage locations of a second register and to store duplicates of the plurality of non-contiguous groups of the source bits into groups of destination storage locations of the second register adjacent to the non-contiguous groups of destination storage locations.

136. (New) An apparatus comprising:

a plurality of registers;

a core coupled with the registers, the core in response to a first instruction, which indicates operands consisting of a single source operand and a single destination operand, to store a plurality of non-contiguous groups of source bits of the source operand into a plurality of non-contiguous groups of destination storage locations of the destination operand and to store duplicates of the plurality of non-contiguous groups of the source bits into groups of destination storage locations of the destination operand adjacent to the non-contiguous groups of destination storage locations.

137. (New) An apparatus comprising:

a plurality of registers; and

a core coupled with the registers, the core in response to a first instruction to:

store bits [31-0] of a source, which are not explicitly specified through the first instruction, into bit storage locations [63-32] and [31-0] of a destination register; and

storing bits [95-64] of the source, which are not explicitly specified through the first instruction, into bit storage locations [127-96] and [95-64] of the destination register.

138. (New) An apparatus comprising:

a plurality of registers; and

a core coupled with the registers, the core in response to a first instruction to:

store bits [63-32] of a source, which are not explicitly specified through the first instruction, into bit storage locations [31-0] and [63-32] of a destination register; and

store bits [127-96] of the source, which are not explicitly specified through the first instruction, into bit storage locations [127-96] and [95-64] of the destination register.

139. (New) A processor comprising:

a front end to fetch instructions including a first instruction, a second instruction, and a third instruction, wherein each of the first, second, and third instructions is a different type of instruction; and

a core coupled with the front end to execute the instructions including the first instruction, the second instruction, and the third instruction, wherein

the core is responsive to the first instruction, instruction, which indicates a first source and a first destination register, to store bits [31-0] of the first source into bit storage locations [63-32] and [31-0] of the first destination register and to store bits [95-64] of the first source into bit storage locations [127-96] and [95-64] of the first destination register,

the core is responsive to the second instruction, which indicates a second source and a second destination register, to store bits [63-32] of the second source into bit storage locations [31-0] and [63-32] of the second destination register and to store bits [127-96] of the second source into bit storage locations [127-96] and [95-64] of the second destination register, and

the core is responsive to the third instruction, which indicates a third source and a third destination register, to store bits [63-32] of the third source into bit storage locations [127-96] and [63-32] of the third destination register and to store bits [31-0] of the third source into bit storage locations [31-0] and [95-64] of the third destination register.

140. (New) The processor of claim 139, wherein each of the first, second, and third instructions has a different opcode.

141. (New) The processor of claim 139, wherein the first instruction has a format comprising operand indication fields consisting of a first field to indicate the first source and a second field to indicate the first destination register.